What is claimed is:

1. A circuit for transforming a data input/output format of a semiconductor memory device, the circuit comprising:

a first transmission circuit which is activated when a first test mode signal is enabled, receives n data inputs from n data input ends, and transmits the n data inputs to m memory cells, wherein n and m are natural numbers and m is greater than n; and

a second transmission circuit which is activated when a second test mode signal is enabled, receives n data inputs from the n data input ends, and transmits the n data inputs to the m memory cells,

wherein data that is transmitted to adjacent memory cells of the m memory cells is inputted to different input ends of the n data input ends.

2. The circuit of claim 1 further comprising a command register which receives a command and an address from outside the semiconductor device and outputs the first test mode signal and the second test mode signal according to combinations of the command and the address.

3. The circuit of claim 2, wherein the command register is a mode register set (MRS).

4. The circuit of claim 1, wherein the first transmission circuit comprises m switches which connect the n data input ends with the m memory cells in response to the first test mode signal.

5. The circuit of claim 1, wherein the second transmission circuit comprises m switches which connect the n data input ends with the m memory cells in response to the second test mode signal.

6. A method for transforming a data input/output format of a semiconductor memory device, the method comprising:

enabling a first test mode signal;

receiving n data inputs from n data input ends and transmitting the n data inputs to m memory cells while the first test mode signal is enabled, wherein n and m are natural numbers and m is greater than n; and

receiving n data inputs from the n data input ends and transmitting the n data inputs to the m memory cells while the second test mode signal is enabled,

wherein data that is transmitted to adjacent memory cells of the m memory cells is input to different input ends of the n data input ends.

7.   The method of claim 6 further comprising receiving a command and an address from outside the semiconductor memory device and generating the first test mode signal and the second test mode signal according to combinations of the command and the address.